IV. SCINTILLATOR ELECTRONICS

A. Scintillator Front-End Card (SFE)

A1. Introduction

Fig. IV-1 is a block diagram of the overall Muon Scintillator Front-End System consisting of 6500 channels of Photomultiplier Tube (PMT) signals input to approximately 137 Scintillator Front-End (SFE) modules, each with 48 channels. The SFE modules are housed in sixteen (16) 9U x 280 mm VME crates located in the collision hall. Each crate contains a 680xx processor, a Scintillator Readout Controller (SRC) module, a Scintillator LED Pulser (SLP) module and as many as ten SFE modules. The SFE modules accept and process event data from the interactions and provide an event data buffer for Level 1 accepted events. The SRC collects and further processes Level 1 accepted event data from all SFEs in the crate. The SLP is a test module that is used to pulse the LEDs optically connected to the scintillator counters, producing PMT signals for testing purposes. A summary of SFE specifications is presented in Appendix A.

Trigger data corresponding to hit channels is sent directly from each SFE to the muon Level 1 (L1) trigger system for each 132 ns crossing interval via a 1 Gbit/s serial link [12]. It is expected that the scintillator system will have a 1% occupancy which implies that on average only one channel will be hit every other crossing. Event data is processed and temporally stored for each crossing for as long as 4.7 μs while the L1 trigger decision is made. The L1 muon trigger system processes the scintillator trigger data along with that of other muon subsystems and sends its decision to the Trigger Framework (TFW) which processes trigger data from the entire detector. The SRC module receives timing and trigger information about the L1 accepted events from the MRC and passes it on to the SFE modules. Identification of events temporarily being stored in the SFE is determined by the

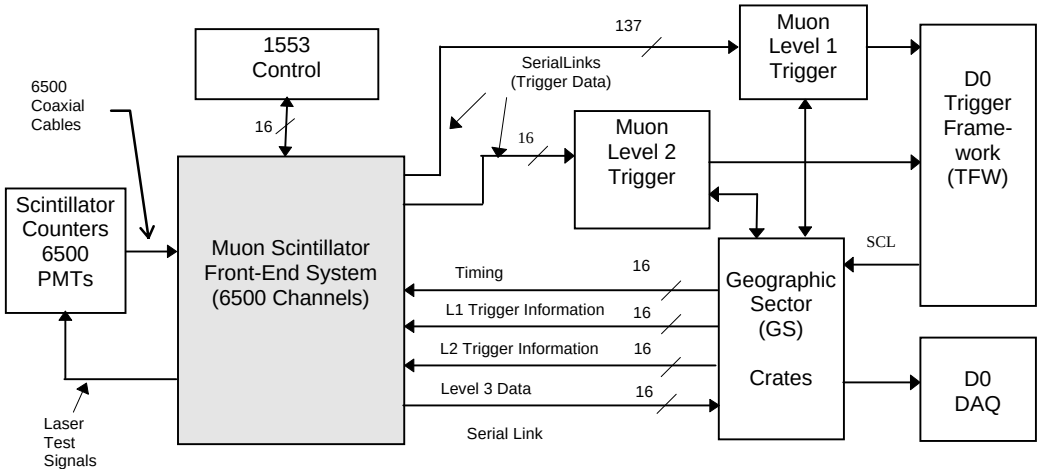

Fig. IV-1. Muon scintillator front-end system.

arrival time of an L1 Accept signal to within one crossing interval. Upon receipt of the L1 Accept, accepted event data is transferred to one of 16 buffer pages of a dual port memory, comprising the SFE L1 Buffer.

Transfer of event data from the SFEs to the SRC is initiated by the SRC immediately following an L1 Accept. The SRC addresses each SFE module in the crate which then outputs its data to one of 16 pages of a dual port memory on the SRC. The dual port on the SRC then serves as an L1 Buffer for the entire crate. After all modules have been read out, the Digital Signal Processor (DSP) on the SRC is notified that the event is ready for readout. The DSP reads, reformats, and transfers selected event data from the SRC L1 Buffer to a Level 2 (L2) trigger data queue for output to the muon L2 trigger system. The DSP awaits the L2 trigger decision from the Trigger Framework and reformats and transfers L2 accepted events to the Level 3 data queue for output to the MRC.

A2. General Operational Description

Fig. IV-2 is a block diagram of the SFE module whose functions are:

- Determine if the channel signal was above threshold and its leading edge occurred within the programmable Timing Gate interval of each crossing (i.e. hit) for the purpose of comprising the L1 trigger data.
- Measure the relative leading edge timing of each hit channel to 1 ns resolution for the purpose of comprising the L2 trigger data.
- Measure the integrated charge input of selected channels during a programmable Analog Gate interval of each crossing for PMT gain monitoring purposes.
- Generate a front panel Trigger - OR signal for the purpose of generating a local test trigger.
- Transmit the hit channel information to the muon L1 trigger system for each crossing that is not within the SYNC GAP interval.
- Store the timing and charge data of each crossing for a programmable period of up to 4.7 μs while an L1 trigger decision is made.
- Maintain an L1 Buffer for the timing and charge data of up to 16 L1 accepted events.
- Output the L1 event data to the crate SRC.

Forty-eight PMT input signals are transformer coupled to high speed amplifiers from which two outputs are derived. The first goes to a two threshold discriminator and the other goes to one of three 16 channel analog multiplexers. One of three programmable timing gates for each group of sixteen channels along with the discriminator outputs are fed to hit logic which produces the trigger OR, L1 trigger data, and scintillator input timing signals. Timing measurement of the input signals are made with four-channel Time Memory Cell (TMC) time digitizer chips developed by Yasuo Arai at KEK National Laboratory for High Energy Physics in Japan [7]. In addition to providing 1 ns timing

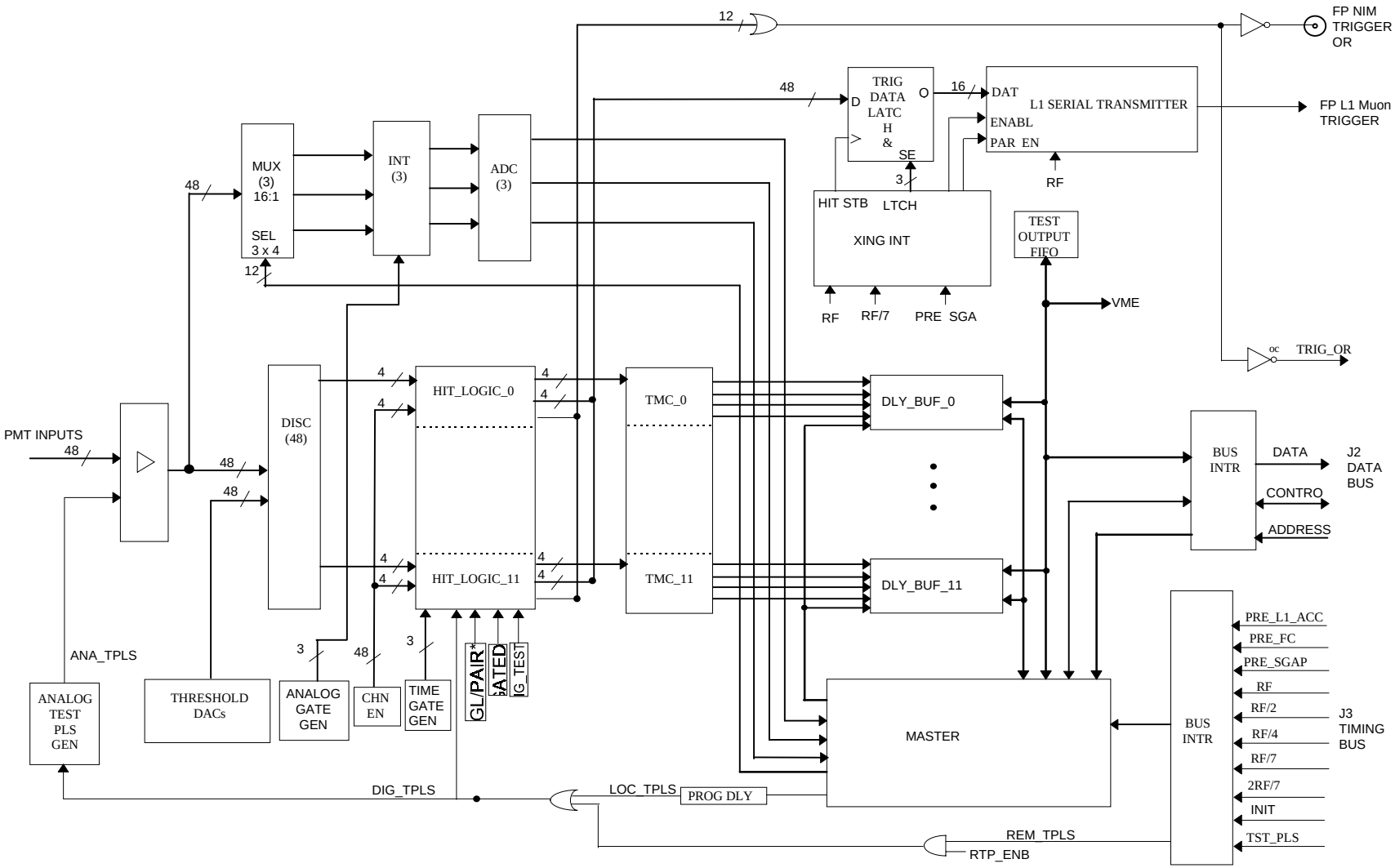

Fig. IV-2. Block diagram of SFE.

measurement data, the TMC also contains a dual port memory capable of temporarily storing the timing data for approximately 4.2 μs at the chosen operating frequency of 4/7 of Tevatron RF. An additional 0.5 μs of temporary storage of the timing data is provided in the Delay Buffer (DLY_BUF) logic to make up the required 4.7 μs temporary storage while the L1 trigger decision is made.

The other amplifier output is used to measure the integrated charge of the input signal on selected channels. For that purpose, the 48 channels are divided into three groups of 16. Each analog multiplexer selects 1 of 16 channels on a fixed basis or in a rotating mode where the channel selection is incremented at the first crossing interval of each turn. Each multiplexer is followed by an integrator and 10 bit analog-to-digital converter (ADC). ADC data is delayed in FIFO memories implemented in the Master Control Logic while the L1 trigger decision is made.

The Master Control logic receives the L1 Accept signal from the SRC and provides control signals to each of the 12 Delay Buffers. TMC timing data of the proper event is transferred to the next available input page of a dual port memory called the L1 Timing Data Buffer implemented in each Delay Buffer PLD. A header word and three ADC data words are implemented in a dual port memory in the Master Controller called the L1 ADC Data Buffer.

Readout of event timing and ADC data on each SFE is initiated by the SRC which establishes an address lock with the Master Controller. The Master Controller then outputs the next in order L1 ADC Data Buffer page consisting of a header word, containing the SFE board address and the corresponding crossing number of the event, followed by three ADC data words. Each ADC data word consists of the selected group number and corresponding data. These four words are output for every event independent of whether or not any channels were hit. The Master Controller then broadcasts the L1 Buffer page to be output and a token pulse to all Delay Buffers who respond on one of 12 dedicated lines if any of their four channels are hit. These dedicated lines are monitored by the Master Controller as well as all other Delay Buffers. Delay Buffer are prioritized by channel number and those having hit channels output one word consisting of channel number and timing data for each hit channel. The Master Controller senses that all data has been read out and ends the address lock with the SRC. The estimate for the readout time for a crate containing 10 SFEs having 1% occupancy is 7.1 μs. The readout time for 100% occupancy is estimated at 47.6 μs.

A3. Analog Input Signal Conditioning

a) Input Signals Characteristics

Photomultiplier input signals are cabled to the front panel of SFE modules over nearly equal 30 foot lengths of RG58 coaxial cable. The PMT side of the cable has isolated BNC connectors having 100 Ω isolation resistors from the shield to HV ground. Connections at the SFE are dual LEMO connectors at the front of the module.

The input signals are negative going exponentially shaped pulses with a sharp leading edge. Inputs come from two different detector regions whose typical pulse characteristics are:

	Pixel Counter	Central C Layer
rise time (10 - 90)	5 ns	8.5
width @ 50%	11 ns	23 ns
base width @ 10%	29 ns	55 ns
fall time (90 - 10)	21 ns	40 ns
maximum peak amplitude	250 mV	250 mV
minimum peak amplitude	5 mV	5 mV
typical peak amplitude	25 mV	25 mV

Although the output amplitude of the PMT signals can be controlled by adjusting their high voltage, it is desired that they operate with the lowest possible value to extend the life of the PMTs. The PMT high voltages are adjustable in groups of sixteen. The variance in input signal arrival time on a given module is expected to be 2 - 3 ns.

b) Input Amplifier Circuit

Fig. IV-3 shows the input amplifier circuit for each channel. The shield of adjacent channels are common within one dual LEMO connector and tied to analog ground via a Zero Ω resistor. This resistor will be omitted in the final assembly if tests show that signal quality is improved by doing so. The 50 Ω termination of the input cable is through two 25 Ω resistors to ground on the secondary of the isolation transformer which has been tested in magnetic field of up to 300 gauss. A common test pulse will be injected to all channels and is discussed further in the following section. The NEC 1663 differential amplifier operating at a gain of 10 has a typical bandwidth of 700 MHz. With a ± 5V power supply, the amplifier has a typical output offset of +2.9V and a maximum output swing of 4V p-p.

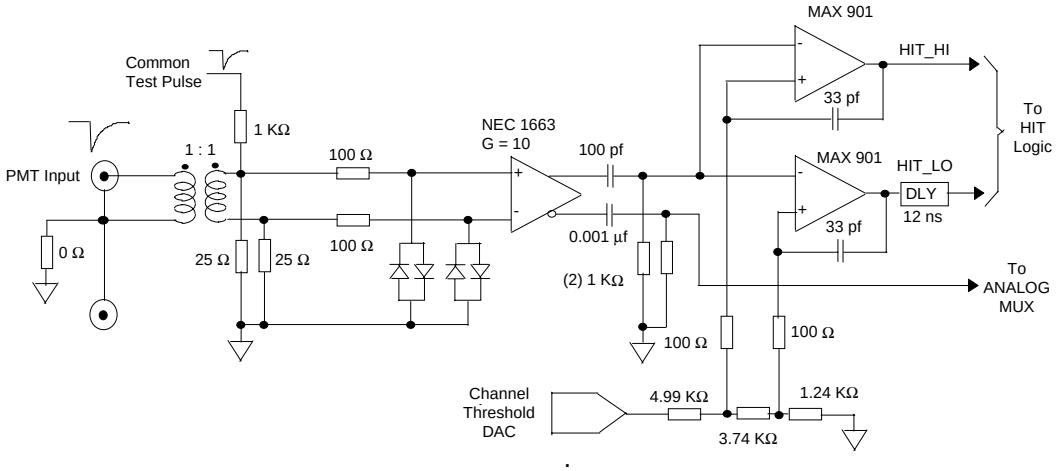

Fig. IV-3. Input amplifier and discriminator.

A ± 6V power source derived from ± 12V is used for power in an effort to increase the linear output swing to at least 2.5 V in one direction. Although the amplifier has a

differential output, the two outputs are used for different purposes. The negative going output is AC coupled to two MAX 901 comparators with an RC time constant of 100 ns and is used for timing measurement. This is chosen to be long enough to preserve the pulse characteristics for timing measurements and short enough to recover the base line between successive pulses (1.32 μs @10% occupancy). The positive going output is AC coupled to an analog multiplexer for charge measurement. The time constant on this output is 1 μs or about 10 times the maximum integration interval. The 33 pf capacitor from the comparator's output to its positive input provides high frequency positive feedback to set a minimum pulse width.

c) Analog Test Pulse Generation

A common analog test pulse is injected into all channels using the circuit in Fig. IV-4 where the source is centrally located and drives a 100 Ω micro strip transmission line feeding each channel. An 8 bit DAC is used to set the amplitude and timing is derived from the DIG_TPL generated locally on the SFE or via the backplane by the SRC.

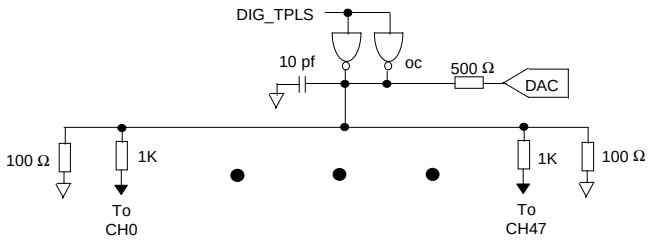

Fig. IV-4. Analog test pulse generator.

d) Discriminator Threshold DACs

The two MAX 901 comparators make up a two level discriminator with the low threshold level fixed at one-fourth of the high threshold level. Each channel has an 8 bit -5V FS output Digital to Analog Converter (DAC) resulting in the following threshold ranges:

	Referred Amplifier Output		Referred to Input	
	1LSB	FS	1 LSB	FS
High Level	-10 mV	-2.55 V	1 mV	-255 mV
Low Level	-2.5 mV	-638 mV	-0.25 mV	-64 mV

A4. Timing Signal Processing

a) Timing Gate Generation

A programmable timing gate pulse is generated within every 132 ns crossing interval which is used to limit the processing of discriminator outputs to those only occurring during the gate period. Three timing gates are generated with each going to the hit logic of 16 channels. Fig. IV-5 shows the logic used to generate the timing gate for which both the

delay and width of the pulse are programmable. A two bit coarse delay setting along with the RF and RF/7 clocks are input to an Altera Programmable Logic Device (PLD) The logic produces a trigger pulse at one of four RF clock edges of the seven RF periods during each crossing interval. This trigger is input to a four bit hybrid programmable delay (DLY 1) having a 2 ns resolution and a maximum delay of 39 ns including a zero step of 9 ns. Because the variable delay range of 30 ns overlaps an RF period of 18.8 ns, two different coarse and fine settings can provide same delay. The output of DLY 1 is input to an RS flip-flop initiating the leading edge of timing gate, TGATE* and to the input of a second programmable delay (DLY2) which controls the width of TGATE*. DLY 2 is a 6 bit device having a 2 ns resolution and maximum delay of 140 ns including a zero step of 14 ns. An erroneous timing gate can be produced if a large width setting causes the timing gate to fall

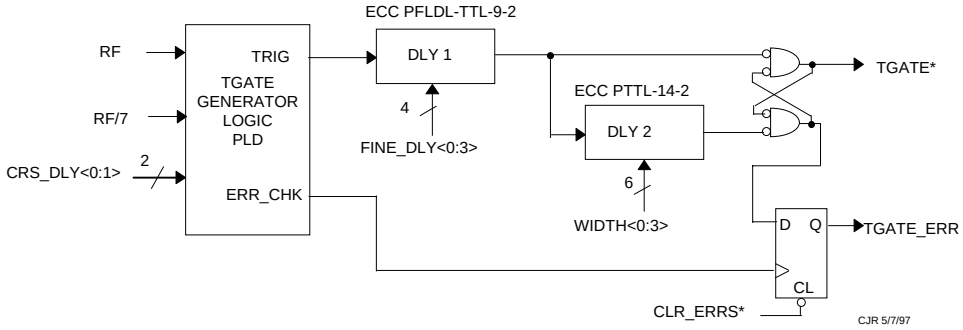

Fig. IV-5. Timing gate generator.

over into the next crossing interval. Should this occur, TGATE_ERR will be latched in a Control and Status Register for diagnostic purposes, but will not effect the SFE operation.

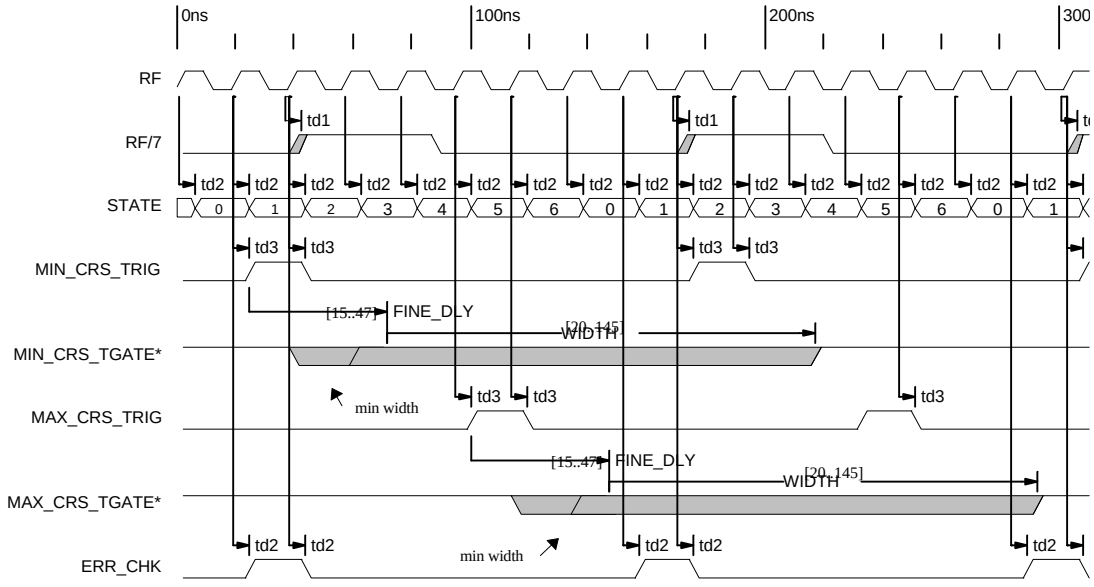

Fig. IV-6. Gate generator timing.

The present design has no hardware limits to prevent this error condition nor is it intended to pass on the error status to the data acquisition system. The TGATE* and TGATE_ERR flip-flops are implemented inside the Crossing Interval Sequencer PLD.

The timing diagram in Fig. IV-6 shows the TGATE* timing for both minimum and maximum coarse delay settings and the possibility of overlapping into the next crossing interval. The estimated fine delay range {15..47} and width range {20..145} that are indicated includes logic propagation delays in addition to the programmable delays. A summary of the timing gate design parameters are listed below. The delay ranges indicated are relative to RF/7 whose phase with respect to the input signals is controlled by the SRC in each crate to a resolution of one RF period.

	DELAY	WIDTH
Coarse resolution	18.84 ns	n/a
Fine resolution	2 ns	2 ns
Accuracy @ 25 °C	±1.2 ns	±2 ns
Minimum	±5 ns	20 ns
Maximum	105 ±5 ns	145 ns
Temperature stability (0 -70°C)	-300 PPM/°C	-300 PPM/°
Power supply variation ±5%	-/+ 1.5%	-/+ 1.5%

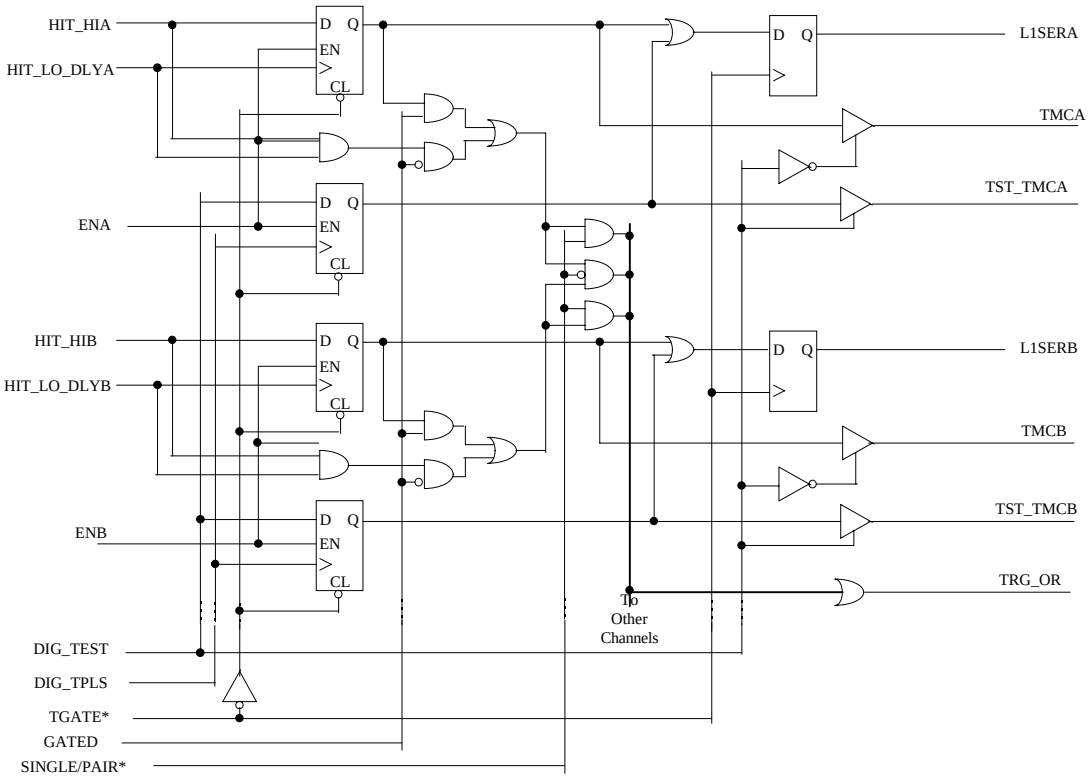

Fig. IV-7. Hit logic of two channels.

b) Hit Logic

Two of the four channels of hit logic implemented in an Altera 7032 CPLD and shown in Fig. IV-7. Hit logic I/Os include:

Per Channel Inputs

- HIT_HI — HIT_HI output of the discriminator
- HIT_LO_DLY — Delayed HIT_LO output of the discriminator
- EN — Channel enable

Per Channel Outputs

- TMC — Timing signal output to TMC wire-ORed with TST_TMC
- TST_TMC — Test timing signal output to TMC wire-ORed with TMC
- L1SER — Logic output to L1 Serial Link logic

Common Inputs

- TGATE* — Timing gate input
- DIG_TPLS — Digital test pulse timing input
- DIG_TEST — Logic input enables selects DIG_TPLS as timing input.
- GATED — Logic input requires TGATE* for TRIG_OR output
- SGL/PAIR* — When high, TRIG_OR output generated by any hit channel. When low, TRIG_OR output generated only if both channels of any channel pair are hit.

Common Output

- TRG_OR — Trigger OR output for the 4 Channels

HIT_LO_DLY is the HIT_LO discriminator output delayed by a fixed amount chosen to exceed the maximum rise time of the signal input. Although a hit on a given channel

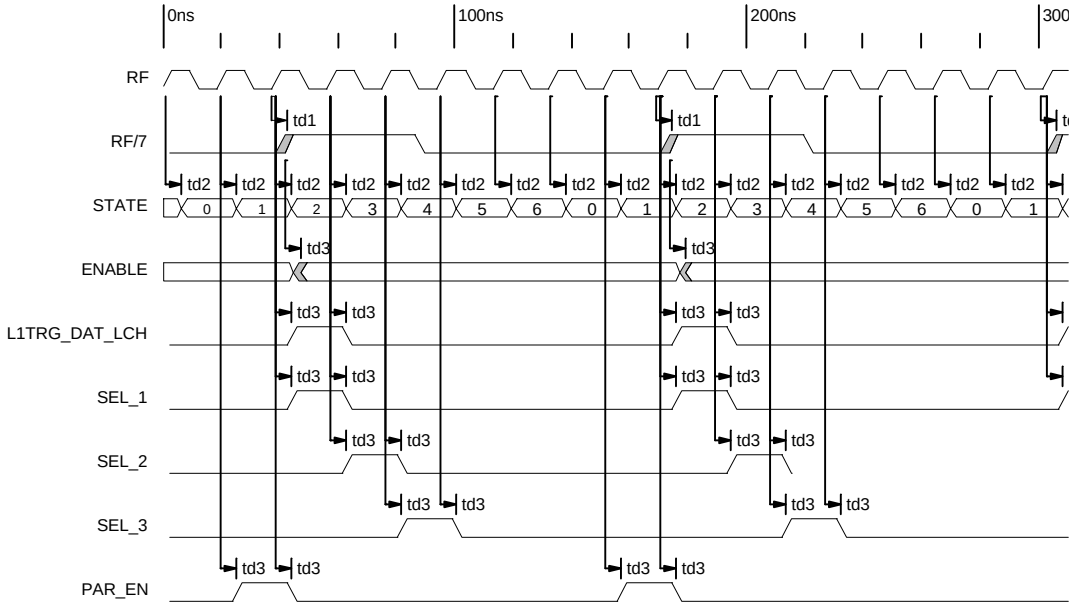

Fig. IV-8. L1 serial interface logic timing.

requires the coincidence of HIT_HI and HIT_LO_DLY, the timing information is determined by the HIT_LO_DLY input.

c) Output to Muon L1 Trigger

The Output to the muon L1 trigger is via a high speed (1 GHz) serial link. The implementation used on the SFE of the Serial Transmitter Daughter Board is described in [12]. The daughter card mounted on the SFE has a coaxial cable output to coaxial bulk head connector accessible from the front of the module. The trigger data consisting of 48 bits of hit channel data are latched into three 16 bit latches at the end of each crossing interval. Using the RF clock as a data strobe, this data is input to the serial transmitter during the first three of seven RF cycles in the next crossing interval. The ENABLE input to the daughter board corresponds to the deasserted state of SYNC_GAP and is derived from clocking the inverted PRE_SGAP signal using the RF/7 clock. Another input to the daughter board is PAR_EN (Parity_Enable) and is generated at the seventh RF cycle of each crossing interval. Fig. IV-8 shows the timing signals produced by the L1 trigger logic implemented in the Crossing Interval Sequencer CPLD.

d) Trigger-OR Output

The Trigger-OR output of the hit logic is the logical sum of hits on enabled channels. Two independent control modes that are common to all SFE channels further determine the nature of the output. In Gated Mode, only hits that occur during the TGATE* interval are summed whereas, in Transparent Mode, hits can occur at any time. In Single Mode, each channel is independent, whereas is Paired Mode, two adjacent channels must both have hits. The TRG_OR output of each of the 12 hit logic PLDs is summed, converted to a NIM level and output at the front panel via a LEMO connector. In addition, the sum is also inverted and output to the backplane using an open collector driver. This bussed wire-OR signal is used locally by the SRC to generate the L1 Accept after issuing a test pulse. There are two available test pulse sources for the SFE card. In Remote Test Pulse mode, channel hits arise from an internal SFE test pulser. When disabled, the Scintillator LED Pulser (SLP) module can be used to drive an external LED flasher to simulate scintillator light at the PMT photocathode.

e) TMC Time Digitizer

Timing measurements of the input signals are accomplished with twelve four-channel custom TMCTEG3 time digitizer chips. The TMC has several modes of operation that are described in [13]. Only mode 0 is used by the SFE. Although the TMC is run with RF/7 as the clock input, timing measurements are made relative to an internal PLL clock of 4•RF/7 (30.3 MHz). Time resolution is determined by dividing each 4•RF/7 period (33 ns) by 32 resulting in timing resolution measurement of 1.03 ns.

The leading edge timing of the TMC output of the hit logic represents the PMT input or the input test pulse arrival time, whereas the TST_TMC output represents the timing of the common digital test pulse. Each channel's TMC and TST_TMC signals are wire ORed and input to the TMC. Because these signals are latched in the hit logic, only one leading edge can occur during a crossing interval. The TMC produces a hit bit plus five bits of timing data corresponding to the arrival time of the leading edge of the input during any of the four PLL clock periods of the crossing interval. The output of a separate two bit coarse

time counter driven at the same rate as the PLL clock is appended to the five bits of TMC data, providing a continuous 1 ns resolution over the entire crossing interval.

f) L1 TDC Pipeline

In addition to the time digitizer section, the TMC contains a 6 bit by 128 location dual port memory for each channel. The TMC timing data is written to the dual port configured as a FIFO on each PLL clock cycle which also increments both its read and write pointers. By initializing the read and write pointers with a given offset, the dual port performs as a programmable depth FIFO. With 128 locations, the dual port can hold the TMC data for a period of 128 x 33 ns = 4.2 μs. Because the L1 trigger latency can be larger then 4.2 μs, an additional delay is implemented in the form of a six wide by 16 deep shift register adding another 16 x 33 ns = 528 ns for a total trigger latency delay of 4.73 μs. Depth programmability of the overall delay will be via the initial offset of the TMC's read and write pointers.

Delay Buffer CPLD has a shift register accepting data from its corresponding TMC channel. The shift register is clocked by the TMC's write strobe output (WS*) which runs at the 30.3 MHz PLL clock rate. Two bits of common coarse time are produced in the Master Control CPLD and input to each Delay Buffer. The six bit output of the shift register plus two bits of coarse time are clocked into a holding latch by WS*. The common HIT_EN input to the Delay Buffer is also produced in the Master Control CPLD and goes high during the crossing interval after the receipt of the L1 Accept signal (PRE_L1ACC). The HIT_EN is combined with the hit bit output of the timing data holding latch to disable further clocking of the latch. As a result, the coarse time and TMC data corresponding to the first rising edge during a crossing interval is captured in the holding latch awaiting transfer to the L1 Timing Data Buffer.

g) L1 TDC Data Buffering

The L1 Timing Data Buffer is implemented in a 12 bit by 64 location dual port memory configured within the Delay Buffer. The dual port is divided into 16 pages of four locations, where each location contains the TMC timing data of one channel. The latched TMC data in the holding latch is input to the dual port via the 4:1 MUX in the four RF/4 (13 MHz) cycles following the L1 Accept. This is followed by the HIT_CLR* signal clearing the data in the holding latch making it ready to accept the next event. Although another event could be accepted after four crossing intervals or 528 ns, the minimum time between L1 Accepts is expected to be 2.6 μs. There is a counter used to determine the input page and is incremented after the event data has been stored in the dual port memory. All of the control signals used to transfer the data to the dual port memory are generated in the Master Control CPLD and distributed to each Delay Buffer.

A5. Analog Signal Processing

The analog signal processing consists of measuring the integrated charge input from selected channels for the purpose of monitoring PMT gain variations over time. The 48 channels are divided into three groups of 16 to allow three channels to be monitored at any given time. The positive going output of the input amplifier circuit shown in Fig. IV-9

goes to one of three analog multiplexers that select one of 16 channels to be monitored. Each multiplexer is followed by an integrator and a 10 bit ADC. Its data is delayed in FIFO memories implemented in the Master Control Logic while the L1 trigger decision is made. A 16 page dual port is also implemented in the Master Control PLD and serves as the L1 ADC Data Buffer.

a) Analog Gate Generation

Three analog gates (AGATE) are generated for use by the corresponding group of 16 channels. It is intended to implement the three analog gates in the same manner with the same specifications as timing gate generators described in section A4.

b) Analog Multiplexer Channel Selection

Channel selection of each multiplexer is determined by a four bit counter output from the Master Control CPLD which runs in either a fixed channel mode or in a rotating channel mode. In fixed mode, channel selection is downloaded in VME and the counter is updated at the trailing edge of the FIRST CROSSING interval. In rotating mode channel selection is incremented in a rotating manner at trailing edge of the FIRST CROSSING interval. FIRST CROSSING is used for this purpose to allow for settling time because it occurs in the SYNC GAP when no events are to be accepted.

c) Gated Integrator

The gated charge integrator circuit shown in Fig. IV-9 is based upon a similar circuit used in the PDT electronics and is discussed in [14]. Integrator gain is determined by the 510 Ω input resistor and the 50 pf integrating capacitor. It is anticipated that values for these components will be selected empirically for best performance. Gain will be determined by Central C Layer signal characteristics such that they yield a +1V full scale output corresponding to the full scale range of the ADC. The AD712 low frequency integrator provides feedback to maintain a zero baseline. The gating interval for each group of 16

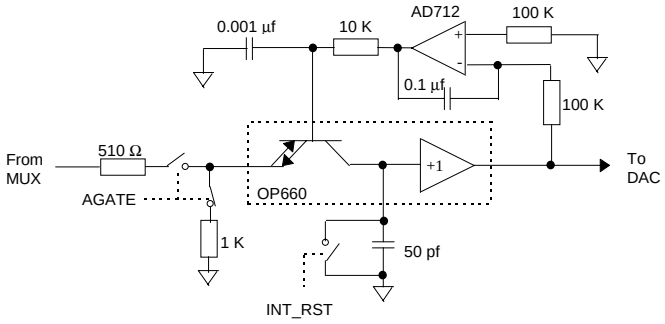

Fig. IV-9. Gated integrator.

channels is determined by a corresponding analog gate signal, AGATE. The integrator reset signal, RST_INT, is common to all 3 integrators and is produced at the end of each crossing interval. RST_INT is implemented in the Gate Generator CPLD and is firmware programmable to two RF periods or 38 ns.

d) Analog to Digital Converter

The AD876 is a 10 bit 20 MSPS ADC that has an on chip sample and hold. The device uses a multistage architecture where the conversion takes place over 3.5 clock cycles (see Fig. IV-10) which makes up part of the L1 trigger latency analog data storage. The nominal input range of the ADC is +2 V to +4 V. The integrator output is amplified by a factor of two and offset by two volts to match the input range of the ADC using an AD818 Op Amp. Reference inputs to the ADC are provided by AD826 Op Amps with an AD586 reference voltage source. OP Amps with high speed and high drive capability were selected to drive the ADC signal and reference inputs to minimize settling time due high capacitive loading by the ADC. Fig. IV-10 shows the crossing interval timing signals that are generated for analog signal processing. RST_INT is used in place of ERR-CHK in Fig. IV-5 to latch a corresponding analog gate error condition.

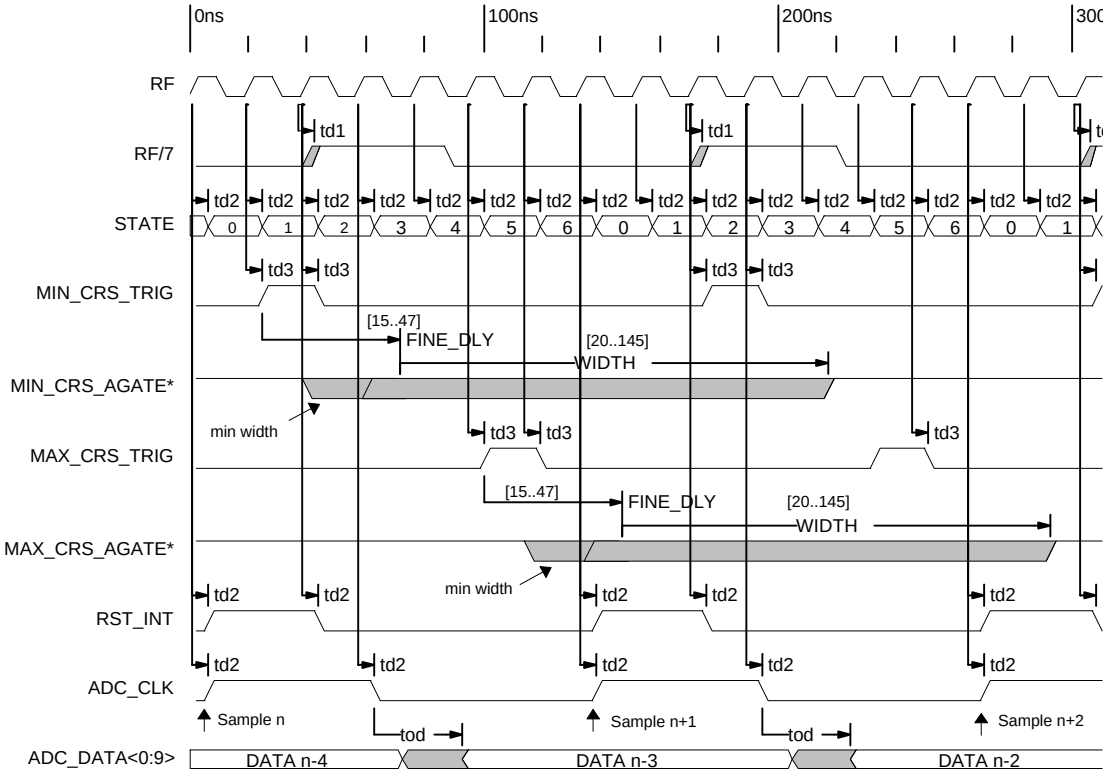

Fig. IV-10. Analog crossing interval timing.

e) L1 ADC Pipeline

A programmable depth FIFO implemented in the Master Control PLD plus the four stage pipeline architecture of the ADC is used to store the analog data while the L1 trigger decision is made. A 30 bit wide ADC Delay FIFO delays the data from all three ADCs and is shown in Fig. IV-11 which contains the VME interface used to download several control parameters, one of which is ADC_DEL<5:0> that is used to program the depth of the FIFO. The maximum total delay including the ADC pipeline is 8.8 μs.

The Master Control CPLD contains a crossing counter that is preset (if needed) at the FIRST CROSSING of each turn. The crossing counter is preset to such that it lags the real time crossing number by the value of the trigger latency in crossing intervals. For example if the L1 trigger latency was 35 crossing intervals x 132 ns = 4.6 μs , the crossing counter would be preset to 160 - 35 = 125. When the L1 Accept is received, the crossing counter, XING<7:0>, equals the event crossing number.

In fixed channel mode, the three ADC group channel numbers are input to the Master Control PLD from VME and loaded into the corresponding counter at the interval following FIRST CROSSING. In rotating channel mode the counter is incremented on each at FIRST CROSSING. The counter value is latched by CHAND_X<3:0> when XING<7:0> = 1 and directly output to the analog MUX. This latched value then changes at the same time that the corresponding ADC data is output from the ADC Delay FIFO. If the crossing corresponded to an accepted event, both ADC data and channel number would be latched for transfer to the L1 ADC Data Buffer.

f) L1 ADC Data Buffering

Fig. IV-11 contains the ADC data holding latch and the logic to control the transfer of the ADC data as well as the TMC timing data to their respective dual ports serving as the L1 Timing Data Buffer. The L1 ADC Data Buffer is a 16 bit wide by 64 location dual port divided into 16 buffer pages. The first location of each page contains that event header word and the other three locations contain the ADC data. Transfer from the analog data holding latch to the dual port is identical to the timing data transfer discussed in Section A4.

A6. Data Output Logic

Transfer of event data from the SFEs to the SRC is initiated by the SRC which successively addresses each SFE module in the crate. After an address lock between the SRC and an SFE is established, the SFE outputs its data to the SRC at a 13 MHz (RF/4) rate. Data is transmitted along a bussed J3 backplane using ABT technology TTL drivers. The Master Control CPLD and Delay Buffers interact to output the event data. The readout functions of these devices are:

Readout Functions of Master Controller

- Control addressing handshake with SRC
- Output header word from 2-Port L1 ADC Buffer to SRC
- Output 3 ADC data words from 2-Port L1 ADC Buffer to SRC
- Output TOKEN to all Delay Buffers
- Monitor HIT_SUM<11:0> (HIT_ORn of all Delay Buffers) to determine when all Delay Buffers have finished outputting their data to the SRC
- Output DONE to SRC and increment output page pointer
  Readout Functions of the Delay Buffer
- Upon receipt of TOKEN, assert HIT_ORn if any of its 4 channels have hit data

- Monitor HIT_SUM <11:0> composed of HIT_ORn of lower order Delay Buffers
- Output TMC Timing data and channel number of hit channels from L1 Timing Data Buffer
- Deassert HIT_ORn when done

Although the header word and ADC data are output for every event, timing data is zero suppressed. The format of the SRC event is shown in

Fig. IV-12. The first event data word shown is the crate word count and is determined by the SRC. Each word output by the SFE has a two bit Data Type at D<15:14>. Board header words are generated primarily for diagnostic purposes and include the board address (BRD_ADR<3:0>) used by the SRC to address each SFE and the L1_XING<7:0> which is the crossing number of the accepted event.

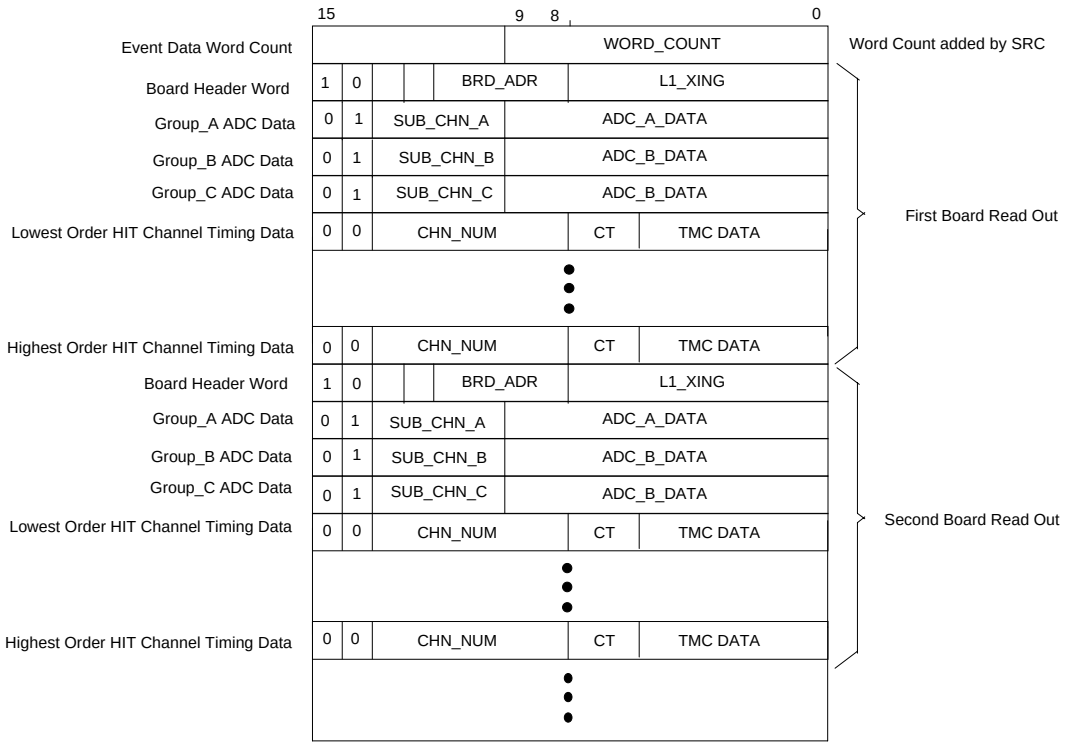

Fig. IV-11. Event readout format.

The readout process begins when the SRC asserts the board address, BRD_ADR<3:0>, along with address enable, ADR_EN. If BRD_ADR matches its DIP switch set board address, the Master Control enables the SFE output drivers by asserting OUT_EN*. The Master Control then output the header word followed by the three ADC data words along with a corresponding data strobe, STBB*. The Master Control sends a token to all Delay Buffers who assert HIT_ORn if they have any channels with hit data. Delay Buffers are prioritized by board wiring such that the lowest order channels are the first to output their timing data and corresponding six bit board channel number. After those Delay Buffers having hit channels have finished sending their data, they deassert their HIT_OR. Upon

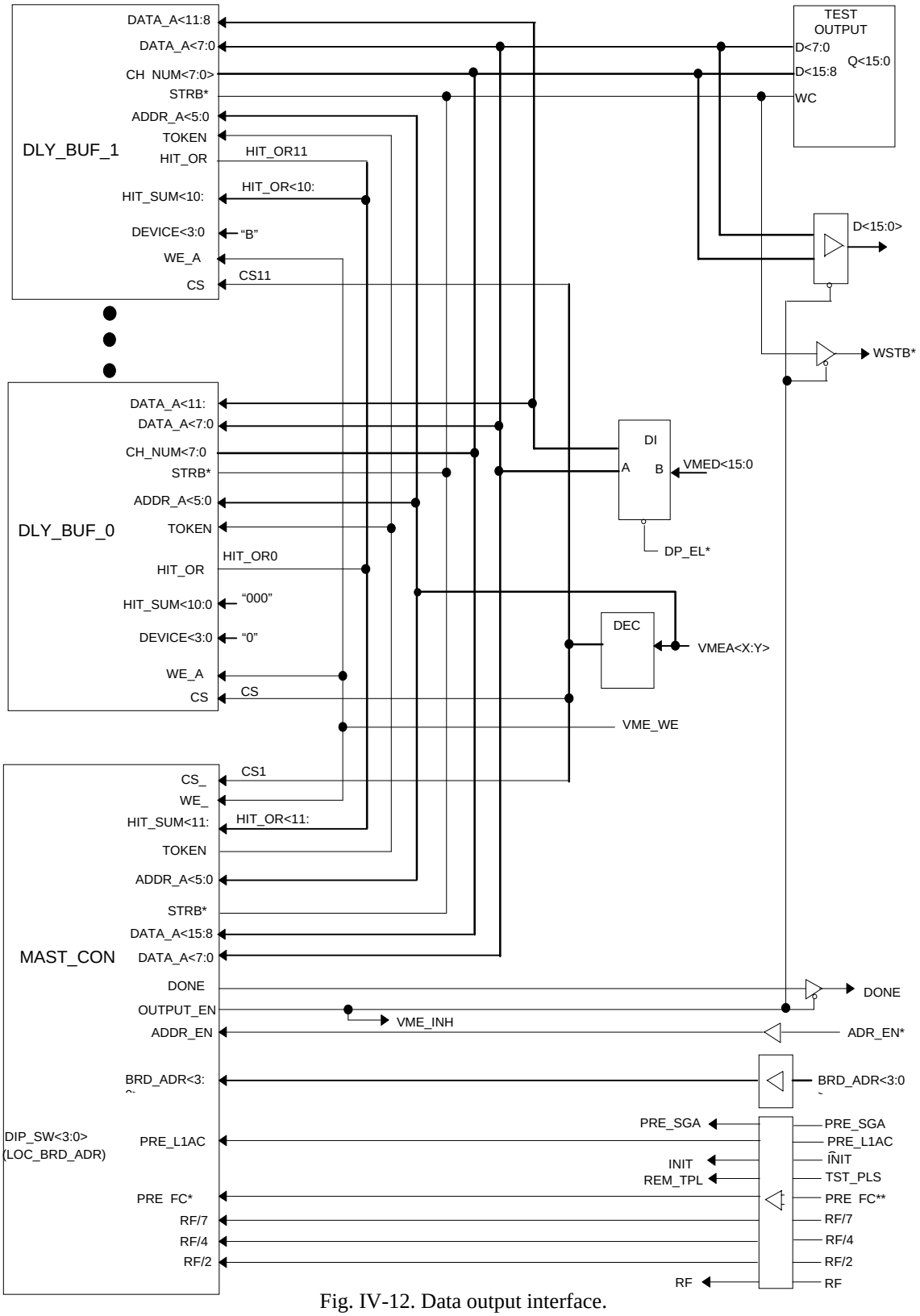

Fig. IV-12. Data output interface.

seeing all HIT_ORs deasserted, the Master Control increments the L1 Buffer output page PGO, deasserts OUT_EN* disabling the output drivers, and asserts DONE back to the SRC.

A7. Test Features

PRE_FC, RF, RF/7, 2RF/7, RF/2, and RF/4 Clocks are supplied by the SRC or a test module.

a) L1 Buffer Memory Test

1) Write and Read Test pattern data to L1 Buffer memory via VME

b) Circular readout of L1 Buffer

1) Download 16 pages of timing data, ADC data, and header data into respective L1 Buffers (dual ports) of each SFE via each SFE's VME interface.
2) Set SFE to inhibit all writes to the dual port RAM from TMCs, ADCs, and Header Latch by disabling all channels.
3) SRC issues PRE_L1ACC or just begins readout. One event's worth of data from one or more SFEs are readout by SRC and compared to expected data.
4) Test Output FIFO on each SFE can be read and compared to data read from SRC.
5) Subsequent PRE_L1ACCs read data from consecutive buffer memory pages in a circular manner.
6) Individual SFEs can be tested by initiating a readout under VME control and reading the Test Output FIFO (VME issued L1ACC and readout has not yet been designed).

c) Read TMC test pattern data

1) Load all TMC dual ports with test pattern data (i.e. 5's A's 0's 1's) plus hit bit. Disable data input to all TMC channels of each SFE by disabling all channel.
2) SRC issues PRE_L1ACC. One events worth of data from one or more SFEs are readout by SRC and compared to expected data.
3) Test Output FIFO on each SFE can be read and compared to data read from SRC.
4) Individual SFEs can be tested by issuing L1ACC and initiating a readout under VME control and reading the Test Output FIFO.

d) Analog Test Pulse Under SRC Control

1) SRC issued test pulse timing that is programmable with a resolution of 2 ns at any crossing interval in a turn. The test pulse rate is limited by a prescaling the number of turns between test pulses from 1 to 65536 or a minimum rate of less then 1 Hz.
2) SRC issues PRE_L1ACC at appropriate time considering L1 trigger latency.
3) Amplitude of test pulse is controlled by SFE VME.
4) Channel enabling, discriminator threshold levels, and timing gate settings determine what channels are read out.
5) Output to Muon L1 trigger occurs.
6) SRC reads out event.

e) Analog Test Pulse Under SFE VME Control

1) With Digital Test Mode of hit logic disabled, a one-shot local test pulse is generated within any VME programmable crossing interval. Coarse delay resolution of 18.8 ns, and fine delay resolution of 2 ns over a 31 ns.
2) One-shot TST_L1ACC generated at VME programmable crossing interval following local test pulse.
3) Amplitude of test pulse is controlled by SFE VME.
4) Pulse amplitude, channel enabling, discriminator threshold levels, and timing gate settings determine what channels are read out.
5) Output to Muon L1 trigger occurs.
6) Test Output FIFO can be read and compared to expected data.

f) Digital Test Pulse Generation Under SFE VME Control

1) With Digital Test Mode of hit logic enabled, one-shot local test pulse is generated within any VME programmable crossing interval. Coarse delay resolution of 18.8 ns, and fine delay resolution of 2 ns over a 31 ns.
2) One-shot TST_L1ACC generated at VME presettable crossing interval following local test pulse.
3) Channel enabling, and timing gate settings determine what channels are read out.
4) Output to Muon L1 trigger occurs.

Test Output FIFO can be read and compared to expected data.

A8. Reference Timing Signal and Clock Distribution

Reference Timing signals and various clocks are generated on the SRC and distributed to all SFEs with Low Voltage Differential Signaling (LVDS) technology along flat cable using the A and C rows of J2. One or more grounded wires on the cable bus separate each signal pair for the purpose of reducing crosstalk. Bussed timing signals include:

Clock Signals	Frequency	Timing Signal	Frequency
RF	53.1 MHz	PRE_FC	47.7 kHz
RF/2	26.6 MHz	PRE_SGAP	47.7 kHz
RF/4	13.3 MHz	PRE_L1ACC	n/a
RF/7	7.6 MHz	TST_PLS	n/a
2RF/7	15.2 MHz	INIT	n/a

Although INIT is not a timing signal and has no current use in the SFE design, it is carried on this bus because of its relationship to PRE_FC and possible future use. PRE_FC, PRE_SGAP, and PRE_L1ACC all are retimed by RF/7 on the SFE to produce FC, SGAP, and L1ACC, respectively. The SRC adjustment resolution of these timing signals and the RF/7 and two RF/7 clocks relative to the beam is one RF period over a minimum range of 300 ns. The SFE requires 50 ±5% duty cycle clocks hence, the RF/7 and 2RF/7 clocks are regenerated using a MC88915 PLL clock driver on the SRC. The cable bus skew across 12 SFE slots is measured at 3.1 ns with a jitter of less than 1 ns pp.

A9. VME Interface

Each crate contains a 680xx processor for parameter downloading, process monitoring, and diagnostic purposes, it does not participate in the data acquisition process. Because the scintillator crates are located in the collision hall, remote access to the 680xx is available via a 1553 interface. Therefore, a remote terminal interface is implemented on the SRC. This interface interrupts the 680xx which then fetches the download information via the SRC's VME slave interface.

The VME interface is implemented using an Altera 7000 series CPLD to provide low level VME functions and an Altera Flex 10K device for address decoding and control logic. Functions of the VME interface on the SFE include:

Control and Status Register bits

- Reset Board (pulse)
- Clear Errors (pulse)
- Reset TMC (pulse)
- Digital Test Mode (R/W)
- Trigger OR Gated/Trans* Mode (R/W)
- Group A Timing Gate Error (R)
- Group B Timing Gate Error (R)
- Group C Timing Gate Error (R)
- Coarse Time Counter Error (R)
- Output FIFO Empty (Read Only)
- Remote Test Pulse Enable
- Reset Output FIFO (pulse)
- Reset ADC FIFO (pulse)
- Test Pulse enable (pulse)
- Configure Flex (pulse)
- Trigger OR Single/Pair* Chan Mode (R/W)
- Group A Analog Gate Error (R)
- Group B Analog Gate Error (R)
- Group C Analog Gate Error (R)
- Crossing Counter Error (R)
- Configure Time Out Error

Three Timing Gate Registers (16 bit R/W)

- 2 bits coarse delay - 18.8 ns resolution
- 4 bits fine delay - 2ns resolution
- 6 bits width - 2ns resolution

Three Analog Gate Registers (16 bit R/W)

- 2 bits coarse delay - 18.8 ns resolution
- 4 bits fine delay - 2ns resolution
- 6 bits width - 2ns resolution

Crossing Number L1 Latency Preset (8 bits R/W)

ADC FIFO Delay (6 bit R/W)

Three ADC Channel Select (5 bits R/W)

- 4 bits group sub-channel select
- 1 bit enable rotating mode

L1 Buffer Page (8 bit Read only)

- 4 bits Input Buffer page - PGI
- 4 bits Output Buffer Page - PGO

Test Pulse Amplitude (8 bits R/W)

Test Pulse Timing (14 bit R/W)

- 8 bit crossing interval
- 2 bits Coarse Delay
- 4 bit Fine Delay

Test L1ACC Crossing Number (8 bits R/W)

Three channel enable Registers (16 bit R/W)

Threshold DAC Control (14 bits R/W)

- 8 bit DAC setting
- 6 bit channel select

TMC CSR (12 bits R/W)

- 8 bit data
- 4 bit TMC select

Dual Port Memory of each L1 Timing Data Buffer (12 bit R/W)

Dual Port Memory of L1 Analog Data Buffer (16 bit R/W)

Output FIFO (16 bit Read only

Flex Configuration Memory (8 bit R/W)

Configuration Init Done (14 bits Read only)

Configuration Status (14 bits Read only)

Configuration Ready (14 bits Read only)

A10. Front Panel Connectors and Displays

Most of the front panel area is taken up by 24 board mounted double LEMO input connectors. A small portion of the available front panel space is taken up by LEDs

a) Front Panel Connectors

Signal Name	Connector Type	Signal Level
• 48 PMT signal inputs	LEMO	analog pulse
• Trigger OR output	LEMO	NIM
• L1 Serial Link	MCX 50Ω?	PECL

b) Front Panel Displays

Module Select LED (Green)

Power On for each voltage if possible (Yellow)

c) Power Requirements

The following are very approximate power requirements:

Voltage	Current	Comment
+5V	3 A	
-5V	25 ma	
+6V	700 ma	Derived from +12V

-6V	700 ma	Derived from -12V
+3.3V	1.1 A	Derived from +5V

A11. In-Circuit Programmability of Programmable Logic Devices

The SFE has fourteen (14) Altera Flex 10K FPGA type programmable logic devices that require configuration at power up. A non-volatile flash memory holds the configuration files which are automatically downloaded to the Altera 10K devices at power up. The flash memory can be rewritten from VME allowing much of the SFE logic to be in-circuit programmable. Several other Altera 7XXX devices including the VME Primitive Interface, hit logic PLDs, and Crossing Interval Sequencer PLD will be in-circuit programmable whenever reasonably possible.

B. Scintillator Readout Controller (SRC)

B1. General Description

Functions of the SRC Module include:

1) Read L1 accepted event data from the SFE L1 buffer of each SFE in the crate into a dual port memory on the SRC having 16 pages of event buffering for the entire crate.
2) Reformat and output L1 accepted event data to the L2 Trigger system via a 160 Mbit/s serial link.
3) Reformat and output accepted L2 event data to the MRC via a 160 Mbit/s serial link.
4) Manage event data transfers based upon receipt of L1 Accept, L2 Accept, and L2 Reject trigger decisions
5) Accept beam timing signals from MRC and provide a means to position timing signals to event data signals at the SFE.
6) Provide 1553 control interface and to provide a download path to the 680xx crate processor.
7) Implement programmable Test Pulse generator.

An on-board timing generator can delay all the arriving timing signals a programmable amount as a means of synchronizing the operation of all SFEs in the crate. For test pulsing, a programmable test pulse generator is fitted.

The SRC uses a Analog Devices 21Csp-01 DSP to control the data acquisition process and has a VME slave interface for control and status read back of various downloaded parameters via the 680xx. Since there is no direct remote access available for the crate 680xx processor, a remote access interface is implemented with a 1553 interface on the SRC. The 1553 interface interrupts the 680xx which then fetches the control or download information via the SRC's VME slave interface.

B2. SFE Readout

One of the major differences between the Proportional Drift Tube and Scintillator systems is the readout of their respective front-end modules. The SRC has a 16 bit by 16K dual port memory organized in 16 pages for the purpose of buffering 16 events with up to100% occupancy of L1 accepted events. In essence, it is an L1 Buffer for the entire crate.Transfer of event data from the SFEs to the SRC begins immediately following an

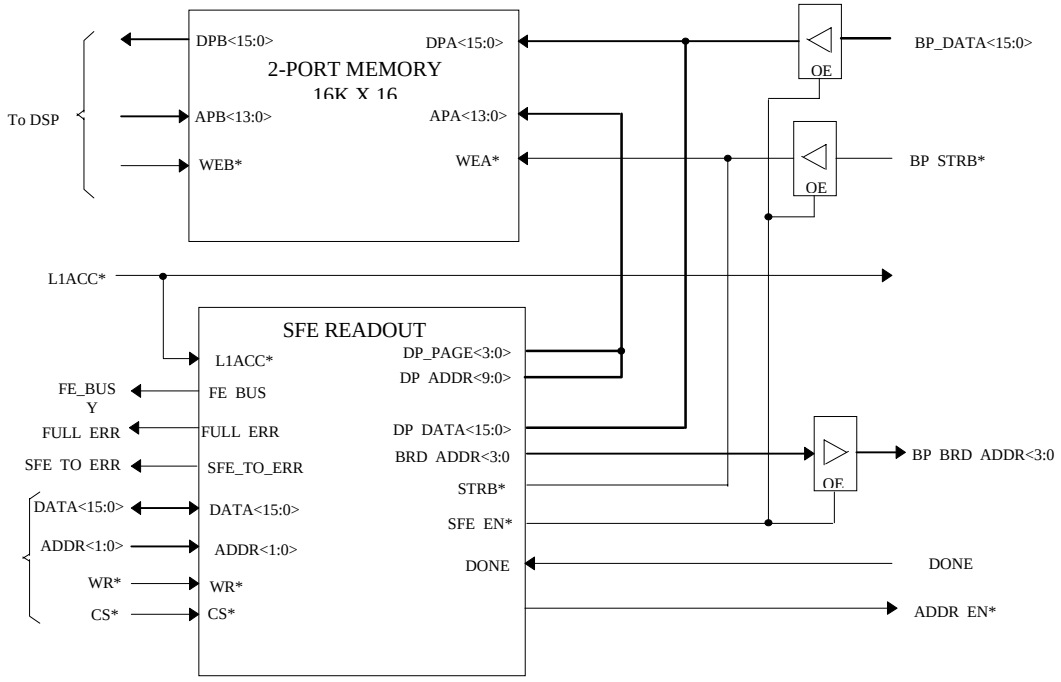

Fig. IV-13. SFE readout interface.

L1 Accept and is entirely controlled by the SFE Readout Control implemented in an Altera Flex 10K10 FPGA. Fig. IV-13 shows the interconnections between the controller and the dual port while Fig. IV-14 shows the definition of various control parameters.Overall control of the readout is provided by the state machine, INP_SEQ, whose state diagram is shown in Fig. IV-15. L1ACC increments a counter called

CONTROL & STATUS REGISTERS

CSR0 Read/Write		
D<15:0>	SFE_MASK<15:0>	Bit map of which SFEs to read out
CSR1 Write		
D<7:0>	TO_SET<7:0>	Timeout Setting 1 LSB = 76 ns
D<15:8>	Not Used	
CSR1 Read		
D<7:0>	TO_SET<7:0>	Timeout Setting 1 LSB = 76 ns
D<11:8>	TO_ERR_ADR<3:0>	Address of first SFE to cause TO error
D12	SFE_TO_ERR	SFE Timeout Error
D13	FULL_ERR	Buffer page has been over written
D<15:14>	Not Used	
CSR2 Write Not Used		
CSR2 Read		
D<15:0>	PG_FULL	Bit map of buffer pages in use
CSR3 Write Not Used		
CSR3 Read		
D<7:0>	L1_COUNT<3:0>	Rolling Counter of L1 Accepts
D<11:8>	DP_PAGE<3:0>	Current or next page 2-Port pointer
D<15:9>	Not Used	

Fig. IV-14. SRC control and status registers.

L1_COUNT and another counter called DP_PAGE which is incremented at the end of the readout of each event. DP_PAGE points to the current or next buffer page to be read out. Each counter is decoded to appropriately set and reset a corresponding bit in a 16 bit register called PAGE FULL whose output called PG_FULL (if non zero) initiates the readout process. A 16 bit readout mask is downloaded to the controller specifying which SFE modules are to be read out. The SFE board address is encoded and output to the J3 data bus along with ADDR_EN*. An address lock between the SRC and an SFE is established by the requirement that the SFE begins to outputs its data within a programmable timeout period. Data is transmitted

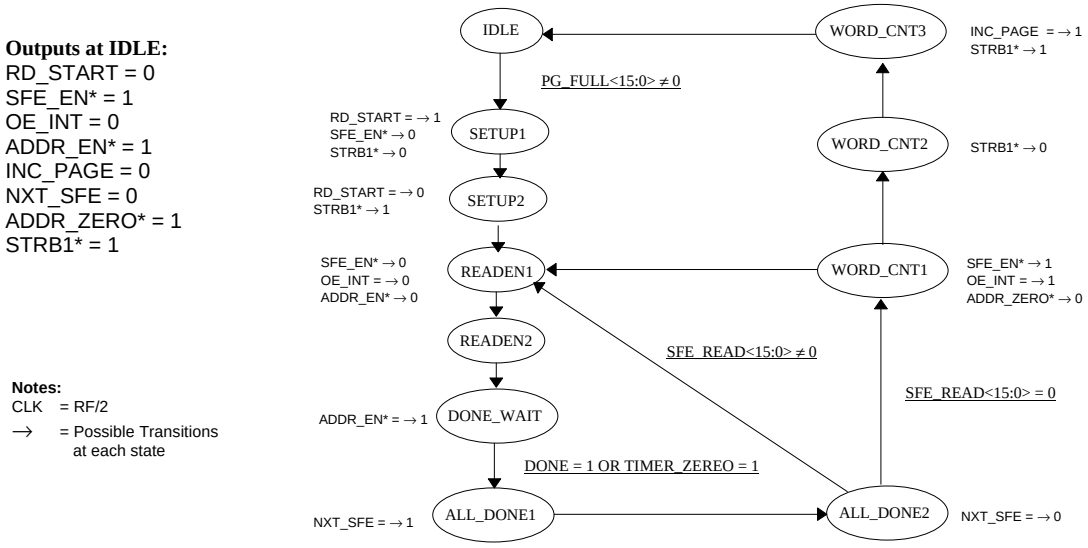

Fig. IV-15. SFE readout controller state machine.

along a bussed J3 backplane using ABT technology TTL drivers with an accompanying data strobe, STRB* at a 13 MHz (RF/4) rate. Data is input directly to the dual port with addressing controlled by the readout controller which also keeps track of the word count. Each SFE sends DONE when all its data has been read out. The controller addresses successive SFEs until all specified SFEs have been readout at which time the controller writes the total data word count at the zero location of the corresponding buffer page. The controller then interrupts the DSP to signify that the readout is done.

Expected readout times for a crate with ten SFEs at various occupancies are:

- 1 % Occupancy - 7.1 μs
- 10% Occupancy - 12.1 μs
- 100 % Occupancy - 47.6 μs

The readout controller asserts FE_BUSY whenever the all 16 L1 buffer pages are in use. If an L1ACC occurs under this condition, the controller asserts FULL_ERR to signify that the readout controller has detected an error. This information will be available through VME for diagnostic purposes only since the DSP will also know of these conditions and determine the appropriate action to take when they occur.

B3. DAQ Control Signals

The signals arriving from the Trigger Framework (TFW) include INIT, L1 Accept, L2 Accept, L2 Reject and eight bits of crossing number associated with a particular trigger decision. The timing of L1 Accept determines which event is accepted and hence transferred to the L1 Buffer on each SFE. L2 Accept and Reject are OR'ed to form a second DSP interrupt. The incoming crossing number is latched by L1 Accepts to be read by the DSP. The crossing numbers of L2 decisions are written into a crossing number FIFO for later reading by the processor during its trigger decision interrupt service routine. These crossing numbers are compared to on-board crossing and turn counters as a check for proper event synchronization. The signals BUSY 1, BUSY 2, ERROR 1, and ERROR 2 are returned to the TFW by way of the MRC when the appropriate condition occurs.

B4. Timing decoder

Timing signals are processed in a manner in the introduction chapter of the this document. For the SFEs, GAP has no relevance and is not used. The RF (53MHz) reference clock which is coming from the TFW SCL board is de-jittered by means of a CY7B991. The RF reference is used to re-phase the RF/7 crossing interval clock before being sent to the SFEs where it is used as the clock for TMCs. These chips allow for a jumper selectable phase adjustment of nine steps of about 1.2 ns each.

B5. VME Interface

The peripherals under VME control include:

a) Serial Ports

One channel of an AM85C30 dual SCC is used as a local RS-232 terminal port and the second channel is setup to use FM encoding with a special double speed clocking mode to attain a speed of 2.5 Mbits/s on a single line for transmit and receive line running to and from the movable counting house. The SRCs do not require a high speed connection, but in the interests of consistency, this SCC is used in all muon sub-systems, including the L1 trigger system, where the bandwidth is useful for downloading large tables.

b) Test Pulse Generator

Separate turn and crossing counters are implemented to allow the adjustment of the timing and repetition rate of test pulses. A 16 bit counter counts turns while a crossing counter counts at the 7 MHz rate and a vernier modulo seven counter runs at 53MHz. A test pulse can be generated at a resolution of 2 ns anywhere within a turn every N turns where N is the prescaled value loaded into the turn counter. To a resolution of 19 ns, counters determine the pulser timing. The finest steps are adjusted by means of a 10 tap 2ns per tap delay line.

c) Timing Generator

It is the responsibility of the TFW to send beam timing information early enough so that the detector with the greatest cable delay will still get the timing information ahead of the actual beam crossings. It is the responsibility of each front-end system to trim the

timing on these incoming signals so that they match the local timing of the interactions. This timing depends on many factors: cable lengths, electronics delays, physical distance from the interaction region etc.

The length of the pipeline delays must be adjusted to match exactly the sum of the propagation delays and the L1 trigger decision time. This cannot be known a priori to the necessary precision and must be trimmed based on measured times. The test pulse

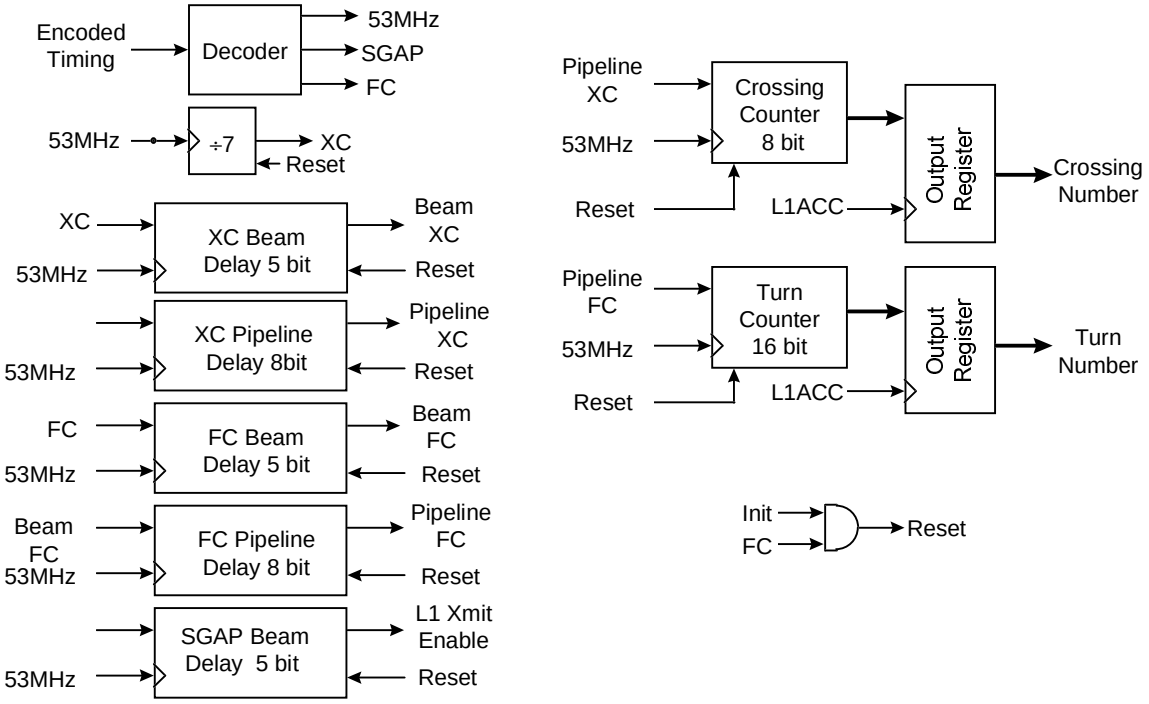

Fig. IV-16. Timing control.

generator can be used to measure the trigger decision time, and thus the value of the pipeline delay. Beam data is used to align the timing sequence to the interactions. For this adjustment, the beam and pipeline delays must be moved together to preserve a fixed relationship between the data emerging from the pipeline and the time of arrival of L1 Accept.

B6. DSP Controller

The DSP is used to control the overall data acquisition process. To that end there are interrupts for trigger decisions and the SFE Readout Done of Level 1 accepted events. The processor chosen is an AD21Csp-01 fixed point DSP processor running at 50MHz. This device is sufficiently powerful to perform almost all data taking (with the exception of the hardware readout) under software control, thus affording a degree of flexibility in the face of changing requirements. It also has the effect of shifting the operational burden from hardware to software. A block diagram of the DSP control logic is shown in Fig. IV-17.

a) Heartbeat

The system reset chip will issue a processor reset if it does not receive a heartbeat input within 300ms. This will obviate the need for remote reset in the event of a software hang. A flag out pin on the processor is attached to the heartbeat pin of the reset chip. There are a number of ways that a heartbeat can be issued. A internal periodic interrupt from the processor's on-chip timer is one possibility.

b) Local Triggering

In order to facilitate local test triggers, the Trigger OR output of each SFE is wire ORed on the data bus. This signal is input to a local delay simulating the timing of the TFW. When this delay is set correctly, there will be no need to modify the timing generator

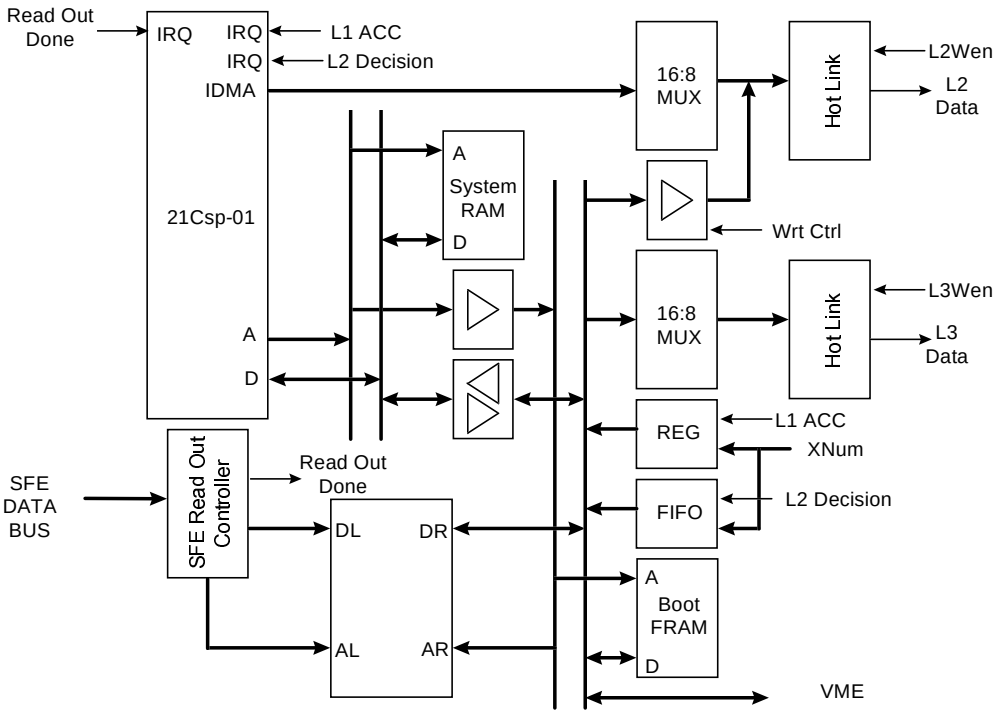

Fig. IV-17. DSP control logic interface.

settings when switching between local triggers and the TFW. An input LEMO for an external trigger is also provided for something like a local scintillator coincidence to be able to trigger a data acquisition routine. Alternatively, this signal could come from a local multi-layer coincidence trigger generated by special tables loaded into the L1 trigger system.

c) Trigger Information Registers

In addition to the crossing number coming from the TFW, on board crossing and turn counters are clocked by appropriately phased copies of the beam orbit timing signals. The processor can immediately check the internal and external crossing numbers for consistency, but because the bandwidth required to ship turn numbers from the MCH

along with the triggers is prohibitively large, the internally generated turn number is sent to the MCH as part of the L3 data block and compared to the TFW generated turn number there.

d) L2 Data Transmission

Each L1 Accept begins the readout process. Once the readout controller has finished writing an event into the Dual Port RAM, the processor must remove the ADC data and reformat the timing data prior to sending it to L2, and arbitrary timing units are normalized to nanoseconds. The IDMA port is used to send L2 data without processor intervention, however, control data must be sent. For this reason, there is an alternate path to the L2 serial transmitter for the specific purpose of sending the Block Begin and Block End control characters required by the L2 data receiver card to detect event boundaries.

e) L3 Data Transmission

The transmission of L3 data is under direct processor control and is presumably a low priority background process, since the expected L3 event rate is 1KHz. No alternate path is needed for control characters in this case. The test and transparent modes of both HOTLink interfaces are controlled by the DSP.

C. Scintillator LED Pulser (SLP).

C1. General Operational Description

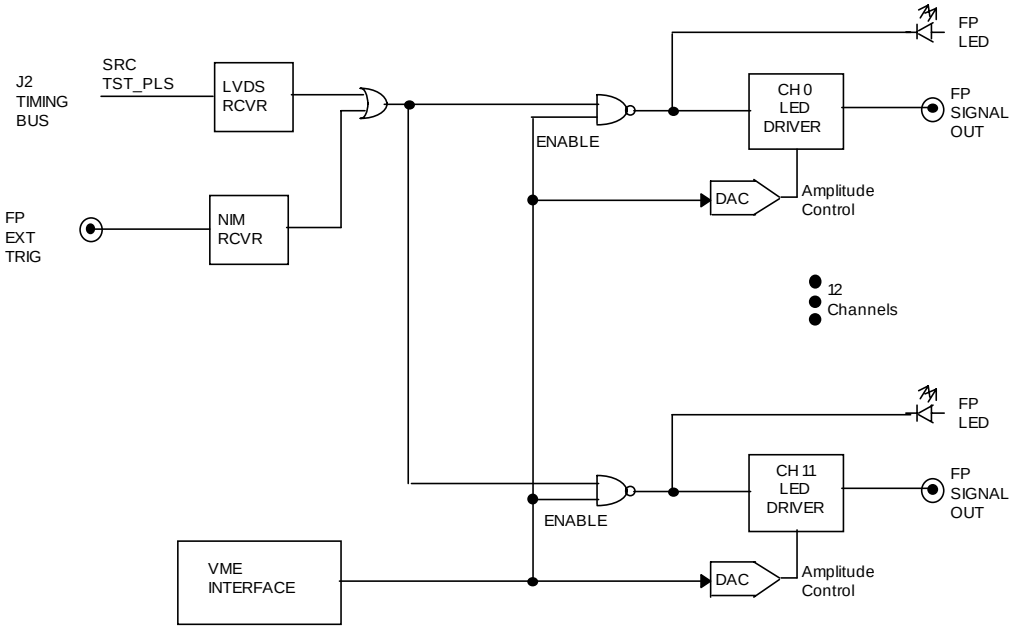

Fig. IV-18. Block diagram of SLP module.

The purpose of the LED pulser is to monitor the long term gain of the PMTs and timing stability of the scintillator system.

Fig. IV-18 is a block diagram of the SLP module whose functions are:

- Accept an LVDS test pulse from the SRC via the backplane.
- Input LEMO front panel NIM external test pulse
- Use logical OR of external input and SRC test pulse as input to 12 channels of LED driver with VME programmable amplitude.
- BNC front panel output of each channel's LED driver signal.
- VME controlled channel enable
- Flash front panel display LED when channel is output.

C2. LED Driver

The LED driver circuit shown in Fig. IV-19 delivers a negative pulse. The amplitude is determined by an eight bit DAC under VME control and has a maximum value of 10 V. The leading edge rise time is expected to be 3 ns at the source but will be significantly larger at the LED depending on the cable length (≈ 50') and its characteristics. The trailing edge decay time is set by an RC time constant of about 25 ns.

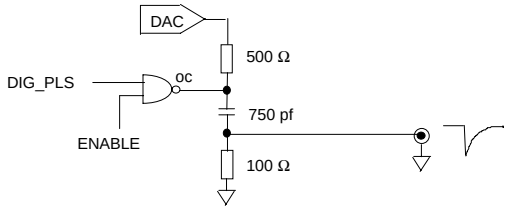

Fig. IV-19. LED pulser circuit.

C3. VME Interface

The VME interface includes the following functions:

- 12 amplitude control registers (8 bit R/W)
- Channel Enable Register (12 bits R/W)

Appendix A.

SFE SPECIFICATION

ANALOG INPUTS

- 48 channel front panel PMT LEMO inputs
- Negative going signal range : - 5 mV to -250 mV (ADC linear range)
- Input termination : 50 Ω
- Each channel individually enabled

HIT DISCRIMINATOR

- Two level threshold discriminator at fixed 4 : 1 ratio
- Individual channel threshold adjustment
- FS high level: -255mV (referred to input)
- High level resolution: -1mV (referred to input)

TIME MEASUREMENTS

- 1.03 ns resolution
- 7 bit binary output over 132 ns crossing interval

ANALOG CHARGE MEASUREMENT

- 10 bit ADC
- One channel from each of three groups is monitored on each crossing interval
- Channel Selection is in a Fixed Mode or Rotating Mode

TIMING GATE

- Three individually controllable gates
- DELAY

  Coarse Resolution: 18.84 ns (1/RF)
  Fine resolution: 2 ns
  Fine adjustment range 31 ns
  Accuracy @ 25°C: ±1.2 ns
  Minimum setting: ±5 ns relative to start of crossing interval (RF/7)
  Maximum setting: 105 ±5 ns relative to start of crossing interval (RF/7)
  Temperature stability (0-70°C): -300ppm/°C
  Power Supply Variation ±5%: -/+ 1.5%

- WIDTH

  Resolution: 2 ns
  Range: 20 ns to 145 ns
  Accuracy @ 25°C: ±2 ns
  Temperature stability (0-70°C): -300ppm/°C
  Power Supply Variation ±5%: -/+ 1.5%
  Note: TGATE ERROR is generated if gate is asserted beyond 113 ns of crossing interval

ANALOG GATE

- Three individually controllable Gates
- DELAY

  Coarse Resolution: 18.84 ns (1/RF)
  Fine resolution: 2 ns
  Fine adjustment range 31 ns
  Accuracy @ 25°C: ±1.2 ns
  Minimum setting: ±5 ns relative to start of crossing interval (RF/7)
  Maximum setting: 105 ±5 ns relative to start of crossing interval (RF/7)
  Temperature stability (0-70°C): -300ppm/°C
  Power Supply Variation ±5%: -/+ 1.5%

- WIDTH

  Resolution: 2 ns
  Range: 20 ns to 145 ns
  Accuracy @ 25°C: ±2 ns
  Temperature stability (0-70°C): -300ppm/°C
  Power Supply Variation ±5%: -/+ 1.5%
  Note: AGATE ERROR is generated if gate is asserted beyond 94 ns of crossing interval

L1 TRIGGER LATENCY STORAGE RANGE

- Programmable from 4 to 36 crossing intervals (528 ns to 4.75 μs)

L1 BUFFER

- 16 events deep

L1 SERIAL LINK OUTPUT

- Hit from all enabled channels at every crossing
- TRIGGER OR OUTPUT
- Single Channel or Paired channel mode select
- Gated or Transparent mode select
- NIM front panel output
- TTL open collector output to L2 timing bus for SRC generation of L1 Accept under test conditions

TEST PULSE GENERATION

- Remote Analog Test Pulse
- Test pulse timing derived externally from SRC
- L1 Accept timing derived from SRC
- Common channel timing ±0.5 ns
- Local Analog Test Pulse
- Test pulse timing VME programmable with resolution of 2 ns in any crossing interval
- L1 Accept timing programmable in any crossing interval

- Common channel timing ±0.5 ns
- Local Digital Test Pulse
- Test pulse timing VME programmable with resolution of 2 ns in any crossing interval
- L1 Accept timing programmable in any crossing interval
- Common channel timing ±0.5 ns

ERROR STATUS BIT

- Error conditions do not inhibit data acquisition

  TGATE ERROR - Timing gate asserted too close to next crossing interval
  AGATE ERROR - Analog gate asserted too close to next crossing interval
  CT ERROR - Coarse Time Counter Error
  XING ERROR - Crossing Counter Error

DATA OUTPUT

- 13 MHz rate
- Readout time at 1 % occupancy: 7.1 μs
- Readout time at 10 % occupancy: 12.1 μs
- Readout time at 100 % occupancy: 47.6 μs

Appendix B:

SRC SPECIFICATION

Processor:

DSP - Analog Devices ADSP21Csp-01 operating at 50MHz

Serial Data Link Rates:

Remote Serial Port Data Rate	- 2.5 Mbits/s
MIL 1553 Data Rate	- 1Mbits/s
L2 Transmission Rate	- 160 Mbits/s
L3 Transmission Rate	- 160 Mbits/s
Encoded Timing Data Rate	- 106 Mbits/s

Timing Generator:

Beam Delay Range/Resolution	- 600/19 ns
Pipeline Delay Range/Resolution	- 4802/19 ns
Test Pulse Delay Resolution	- 2ns
Test Pulse Prescale Range	- 1 to 65535
Internal Trigger Delay Range/Resolution	- 4802/19 ns

Table IV-1. DSP Memory Map

Address(Hex)	Device	No. of Bits
0-1FFF	Internal RAM	24
10000-13FFF	Dual Port RAM	16
14000	L1 Crossing Latch	8
14001	L2 Crossing FIFO	9
14002	Internal Crossing Counter	8
14003	Internal Turn Counter	16
14004	L2 Control Word	9
14005	L3 Data Word	16
14006	Hot Link Control Register	8
18000-1FFFF	External System RAM	24
20000-40000	Boot FRAM	8
Flag Out 0	Busy 1	1
Flag Out 1	Busy 2	1
Flag Out 2	Err 1	1
Flag Out 3	Err 2	1
Flag In 0	Init	1
Flag In 1	L2 Decision FIFO Empty	1

Power Consumption (estimated):

+5V: 5A
-5V: 0.5A

+5VA, -5VA: < 0.1mA

Mechanical: 9U x 280 mm

Front Panel Connectors and Switches:

A 50 pin ribbon cable standard density connector to MRC including:

XING<7:0>	To SRC	Crossing number corresponding to simultaneous assertion of L1ACC, L2ACC, or L2REJ
INIT	To SRC	TFW INIT
L1ACC	To SRC	Level 1 Accept
L2ACC	To SRC	Level 2 Accept
L2REJ	To SRC	Level 2 Reject
TxDAT	To SRC	Serial Data Input
DONE	To SRC	Done processing L3 Data of current event, ready for L3 Data of next event
STRB	To SRC	Strobe for XING<7:0>, L1ACC, L2ACC, & L2REJ
RxDAT	To MRC	Serial Data Output
ERR1	To MRC	Level 1 Error
BUSY1	To MRC	Level 1 Busy, SRC cannot execute L1 Accept
ERR2	To MRC	Level 2 Error
BUSY2	To MRC	Level 2 Busy, SRC cannot execute L2 Accept

A four ribbon coaxial connector including:

Encoded Beam Timing (106 MHz)
RF Reference (53MHz)
L3 Data (160 Mbit/s)
L2 Data (160 Mbit/s)

A nine pin “D” connector for the local terminal port
Two Trompeter Tri-Axial Connectors for the MIL 1553 Connection
A LEMO connector for local trigger out
A LEMO connector for local trigger in
A System Reset Switch

Front Panel LEDs:

+5V,-5V,+5VA,-5VA power indicators
MIL 1553 Remote Terminal Access
MIL 1553 Remote Terminal Timeout

Appendix C.

SLP SPECIFICATION

Number of Channels	12
Pulse Characteristics:	
Amplitude 8 bit DAC	0 to 10v
Leading edge rise time	< 3ns
Trailing edge time constant	25 ns
Polarity	negative
Amplitude stability	<1%
Channel to channel time skew	<1 ns
Mechanical	9U x 280 mm